WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of unit cells constituting a cell array, in which each four unit cells share a contact region and are arranged in an X pattern with said contact region being a center thereof; and

a first bit line for read operation provided on a layer provided over the semiconductor substrate; and

a second bit line for program and erase operations provided on the layer provided over the semiconductor substrate;

wherein said unit cell includes a memory transistor comprising:

first and second diffusion regions provided in the semiconductor substrate and separated from each other;

an insulating film including an electric charge trapping film, formed on the semiconductor substrate and covering a region between said first and second diffusion regions; and

a gate electrode formed on and overlaying said insulating film to constitute a word line electrode; and wherein

at least one of said first diffusion region and said second diffusion region in said each unit cell is shared by other unit cell adjacent to said unit cell; and

said first and second diffusion regions are connected to said first and second bit lines respectively.

2. The semiconductor memory device according to claim 1, wherein programming the unit cell is performed by applying a predetermined

positive voltage to the word line connected to the unit cell to be programmed, applying a positive program voltage to the second bit line connected to said unit cell, and setting the first bit line connected to said unit cell to a ground potential to cause channel hot electrons to be injected into said insulating film of said unit cell; and

wherein erasing is performed by setting the word line connected to the unit cell to be erased to said ground potential, and applying a predetermined positive voltage to the second bit line connected to said unit cell to cause hot holes to be injected into said insulating film of said unit cell to neutralize electric charge in said insulating film of said unit cell.

3. The semiconductor memory device according to claim 1, wherein said insulating film comprises: a silicon dioxide film formed on the semiconductor substrate:

a silicon nitride film formed on and overlaying the silicon dioxide film; and

a silicon dioxide film formed on and overlaying the silicon nitride film.

4. The semiconductor memory device according to claim 1, wherein a surface of said gate electrode comprises a metal silicide layer or surfaces of said gate electrode and said first and second diffusion regions comprise metal silicide layers.

5. The semiconductor memory device according to claim 1, wherein the second bit line is extended from one side to other side of said cell array, and when programming is performed, a positive program voltage

is supplied from both sides of said second bit line in a longitudinal direction, connected to the unit cell to be programmed.

6. A semiconductor memory device including:

a semiconductor substrate; and

a plurality of memory cells constituting a cell array; wherein for each adjacent two memory cells in said cell array, there are provided:

first, second and third diffusion regions formed in said semiconductor substrate and separated from one another;

a first insulating film formed on said semiconductor substrate and covering a region between said first diffusion region and said second diffusion region;

a first gate electrode formed on and overlaying said first insulating film;

a second insulating film formed on said substrate and covering a region between said second diffusion region ands aid third diffusion region; and

a second gate electrode formed on and overlaying said second insulating film;

said semiconductor memory device further comprising:

first to third bit lines provided on said layer provided over said semiconductor substrate and connected via associated contacts to said first, second and third diffusion regions respectively; and

a word line connected in common to said first and second gate electrodes or first and second word lines connected respectively to said first and second gate electrodes;

wherein

a memory cell transistor including said first and second diffusion regions, said first insulating film, and said first gate electrode constitutes a first memory cell; and

another memory cell transistor including said second and third diffusion regions, said second insulating film, and said second gate electrode constitutes a second memory cell.

7. The semiconductor memory device according to claim 6, wherein each of said first and second insulating films comprises an electric charge trapping film.

8. The semiconductor memory device according to claim 6, wherein when programming is performed, a predetermined positive voltage is applied to the word line connected to the gate electrode of a memory cell to be programmed, and a positive program voltage is applied to the second bit line connected to said memory cell to be programmed; and

one of the first and third bit lines connected to said memory cell to be programmed is set to a ground potential, and other bit line is set to a positive program inhibiting voltage.

9. The semiconductor memory device according to claim 8, wherein the second bit line is extended from one side to other side of said cell array, and when programming is performed, the positive program voltage is applied from both ends of the second bit line in a longitudinal direction.

10. The semiconductor memory device according to claim 6, wherein erasing is performed by applying a ground potential or a negative

voltage to the word line connected to the gate electrode of a memory cell to be erased,

applying a positive erase voltage to the second bit line connected to said memory cell to be erased, and injecting hot holes into the insulating film of said memory cell, thereby to neutralize electric charges trapped in the insulating film of said memory cell.

11. The semiconductor memory device according to claim 6, wherein when reading is performed, a predetermined positive voltage is applied to the word line connected to the gate electrode of a memory cell to be read, a ground potential is applied to the second bit line connected to said memory cell to be read, and a positive read voltage is applied to one of the first and third bit lines connected to said memory cell to be read.

12. The semiconductor memory device according to claim 6, wherein when reading the unit cell is performed, a predetermined positive voltage is applied to the second bit line connected to a memory cell to be read as a read voltage, and a ground potential is applied to one of the first and third bit lines adjacent to the second bit line and connected to the diffusion region for a transistor of said memory cell to be read; and wherein

the semiconductor memory device further comprises means for determining whether said memory cell to be read is a programmed cell or an unprogrammed cell according to a magnitude of current flowing between two of the diffusion regions for said memory cell transistor.

13. The semiconductor memory device according to claim 6, wherein said first and second gate electrodes are made up of a polycrystalline

silicon film, and at least one gate electrode of said first and second gate electrodes includes a metal silicide layer on a surface thereof.

14. The semiconductor memory device according to claim 13, wherein at least one diffusion region of said first to third diffusion regions includes a metal silicide layer on a surface thereof.

15. The semiconductor memory device according to claim 6, further comprising an impurity region having a polarity opposite that of said second diffusion region and formed at an end portion of said second diffusion region in the semiconductor substrate immediately under at least one gate electrode of said first and second gate electrodes.

16. The semiconductor memory device according to claim 6, further comprising:

a first impurity region having the same polarity as said second diffusion region and a lower concentration than said second diffusion region and formed at an end portion of said second diffusion region in the semiconductor substrate immediately under at least one gate electrode of said first gate electrode and said second gate electrode; and

a second impurity region having a polarity opposite that of said second diffusion region and formed at an end portion of said first impurity region in the semiconductor substrate.

17. The semiconductor memory device according to claim 15, further comprising an impurity region having the same polarity as any of said diffusion regions and a lower concentration than said diffusion regions and formed in the semiconductor substrate at an end portion of at least one of said first diffusion region immediately under said first gate

electrode and said third diffusion region immediately under said second gate electrode.

18. The semiconductor memory device according to claim 6, further comprising an impurity region having an polarity opposite that of said diffusion regions and formed in the semiconductor substrate at an end portion of at least one of said first diffusion region immediately under said first gate electrode and said third diffusion region immediately under said second gate electrode.

19. The semiconductor memory device according to claim 6, further comprising:

a third impurity region having the same polarity as said diffusion regions and a lower concentration than said diffusion regions, and formed in the semiconductor substrate at an end portion of at least one of said first diffusion region immediately under said first gate electrode and said third diffusion region immediately under said second gate electrode; and

a fourth impurity region having a polarity opposite that of said diffusion regions and formed at an end portion of said third impurity region.

20. The semiconductor memory device according to claim 6, further comprising an impurity region having an polarity opposite that of said diffusion regions in at least one of regions in the semiconductor substrate between an end portion of said second diffusion region immediately under said first gate electrode and said first diffusion region and between an end portion of said second diffusion region

immediately under said second gate electrode and said third diffusion region.

21. A semiconductor memory device comprising:

at least first, second third and fourth diffusion regions provided in four regions located on vertexes of a rectangle in a semiconductor substrate for a cell array region having a plurality of memory cells;

wherein

said first and third diffusion regions are located on a first diagonal line; and

said second and fourth diffusion regions are located on a second diagonal line perpendicular to said first diagonal line;

said semiconductor memory device further comprising:

a first insulating film formed on said semiconductor substrate and covering a region between said first and second diffusion regions, and a first gate electrode formed on and overlaying said first insulating film;

a second insulating film formed on said semiconductor substrate and covering a region between said second and third diffusion regions, and a second gate electrode formed on and overlaying said second insulating film;

a third insulating film formed on said semiconductor substrate and covering a region between said third and fourth diffusion regions, and a third gate electrode formed on and overlaying said third insulating film;

a fourth insulating film formed on said semiconductor substrate

and covering a region between said fourth and first diffusion regions, and a fourth gate electrode formed on and overlaying said fourth insulating film;

a first word line connected in common to said first gate electrode and said second gate electrode;

a second word line connected in common to said third gate electrode and said fourth gate electrode;

a first bit line, provided on a layer overlying said semiconductor substrate and crossing over said first and second word lines, said first diffusion region being connected via a contact to said first bit line;

a second bit line, provided on a layer overlying said semiconductor substrate and crossing over said first and second word lines, said second and fourth diffusion regions being connected via contacts in common to said third bit line;

a third bit line, provided on a layer overlying said semiconductor substrate and crossing over said first and second word lines, said third diffusion region being connected via a contact to said third bit line;

wherein

a memory cell transistor including said first and second diffusion regions, said first insulating film, and said first gate electrode constitutes a first memory cell;

a memory cell transistor including said second and third diffusion regions, said second insulating film, and said second gate electrode constitutes a second memory cell adjacent to said first memory

cell;

a memory cell transistor including said third and fourth diffusion regions, said third insulating film, and said third gate electrode constitutes a third memory cell adjacent to said second memory cell; and

a memory cell transistor including said fourth and first diffusion regions, said fourth insulating film, and said fourth gate electrode constitutes a fourth memory cell adjacent to said respective first and third memory cells.

22. The semiconductor memory device according to claim 21, wherein said cell array includes:

a plurality of sets, each set comprising said first to fourth unit cells in a direction along which said first and third bit lines and said second bit line are extended; and

a plurality of sets, each set comprising said first to fourth unit cells in a direction along which said word lines are extended; wherein

a plurality of pairs of said first and second word lines are provided for said sets comprising said first to fourth unit cells disposed in a longitudinal direction of said bit lines;

the fourth diffusion region of one set and the second diffusion region of other set adjacent to said one set among said sets comprising said first to fourth unit cells disposed in said longitudinal direction of the bit lines are made common;

the first diffusion region of one set and the third unit cell of other set adjacent to said one set among said sets comprising said first to

fourth unit cells disposed in a longitudinal direction of said word lines are made common; and

said first bit line and said third bit line are shared between one set and other set adjacent to said one set in said longitudinal direction of the word lines.

23. The semiconductor memory device according to claim 22, wherein the second bit line is extended from one end to other end of said cell array;

the second bit line is connected to a global program and erase bit line disposed across a bank through first and second bank selection transistors at both ends of said cell array; and

when programming is performed, said bank selection transistors at both ends of said cell array are turned on, and the positive program voltage is applied from both ends of the second bit line.

24. The semiconductor memory device according to claim 21, wherein each of said first and fourth insulating films comprises an electric charge trapping film.

25. The semiconductor memory device according to claim 21, wherein when programming is performed, a predetermined positive voltage is applied to one of the first and second word lines connected to a unit cell to be programmed, and a positive program voltage is applied to the second bit line connected to said memory cell to be programmed; and

one of the first and third bit lines connected to said memory cell to be programmed is set to a ground potential, and the other is set to a positive program inhibiting voltage.

26. The semiconductor memory device according to claim 21, wherein a ground potential or a negative voltage is applied to the word line connected to a memory cell to be erased; and

a positive erase voltage is applied to the second bit line connected to a memory cell to be programmed, to cause holes generated to be injected into the insulating film of said memory cell, and to cause electric charge trapped in said insulating film of said memory cell is neutralized, thereby to perform erasing.

27. A method of controlling a semiconductor memory device comprising a cell array having a plurality of memory cells, in which for each two mutually adjacent memory cells in said cell array, there are provided:

first to third diffusion regions formed in a semiconductor substrate and separated from one another;

a first insulating film formed on said semiconductor substrate to cover a region between said first diffusion region and said second diffusion region, and

a first gate electrode formed on and overlaying said first insulating film;

a second insulating film formed on said semiconductor substrate to cover a region between said second diffusion region and said third diffusion region, and

a second gate electrode formed on and overlaying said second insulating film;

wherein

a memory cell transistor including said first and second diffusion regions, said first insulating film, and said first gate electrode constitutes a first memory cell,

another memory cell transistor including said second and third diffusion regions, said second insulating film, and said second gate electrode constitutes a second memory cell,

said first and second gate electrodes are connected to first and second word lines, respectively, or connected in common to compose a word line,

said first diffusion region is connected to a first bit line disposed on a layer overlying said semiconductor substrate via a contact,

said second diffusion region is connected to a second bit line disposed on said layer overlying said semiconductor substrate via a contact, and

said third diffusion region is connected to a third bit line disposed on said layer overlying said semiconductor substrate via a contact,

said method comprising the steps of:

applying a first positive voltage to the word line connected to the gate electrode of a memory cell to be programmed;

applying a second positive voltage lower than the first positive voltage to the second bit line connected to said memory cell to be programmed for a predetermined period of time as a program voltage; and

setting one of the first and third bit lines connected to said memory cell to be programmed to a ground potential and setting the other bit line to a third positive program inhibiting voltage, thereby to cause channel hot electrons to be injected into the insulating film of said memory cell to be programmed, when programming is performed.

28. The method according to claim 27, further comprising the step of:

applying the second positive program voltage from both ends of the second bit line in a longitudinal direction when programming is performed, the second bit line being extended from one end to other end of said cell array.

29. The method according to claim 27, further comprising the steps of:

applying said ground potential or a negative voltage to the word line connected to the gate electrode of a memory cell to be erased; and

applying the first positive voltage to the second bit line connected to said memory cell to be programmed as an erase voltage, thereby to cause hot holes generated to be injected into the insulating film of said memory cell to neutralize electric charge trapped in said insulating film of said memory cell, when erasing is performed.

30. The method according to claim 27, further comprising the steps of:

applying a fourth positive voltage to the word line connected to the gate electrode of a memory cell to be read, applying said ground potential to the second bit line connected to said memory cell to be read; and

applying a read voltage to one of the first and third bit lines connected to said memory cell to be read, when reading is performed.

31. The method according to claim 27, further comprising the steps of:

applying a fifth positive voltage to the second bit line connected to a memory cell to be read as a read voltage and applying said ground potential to one of the first and third bit lines connected to said memory cell to be read; and

determining whether said memory cell to be read is a written cell or an unwritten cell according to a magnitude of current flowing between two of the diffusion regions for said memory cell to be programmed.

32. A method of manufacturing a semiconductor memory device comprising the steps of:

forming an insulating film on a semiconductor substrate and first and second gate electrodes on said insulating film and forming first, second and third diffusion region diffusion regions by doping an impurity into said semiconductor substrate with said gate electrodes patterned as a mask, wherein said first, second and third diffusion regions, are formed in a first region located on one side of said first gate electrode, a second region located between said first gate electrode and said second gate electrode located on an opposite side to said one side of said first gate electrode, and a third region located on an opposite side to said second region for said second gate electrode, respectively;

forming an impurity region having a polarity opposite that of said diffusion regions at an end portion of said second diffusion region in said semiconductor substrate immediately under at least one gate electrode of said first and second gate electrodes;

depositing an insulating film over the semiconductor substrate and removing the insulating film by etch-back, thereby to form spacers made of the insulating film on side walls of said first and second gates; and

depositing a metal film for silicidation over the semiconductor substrate to form metal silicide layers respectively on a surface of said gate electrode and on a surface of said diffusion region;

wherein a memory cell transistor including said first and second diffusion regions, the insulating film under said first gate electrode, and said first gate electrode constitutes a first memory cell,

a memory cell transistor including said second and third diffusion regions, the insulating film under said second gate electrode, and said second gate electrode constitutes a second memory cell, and

said first and second gate electrodes are connected in common to form a word line,

said method further comprising the steps of:

depositing an insulating film over said semiconductor substrate and opening first to third contact openings at locations in said first to third diffusion regions;

filling a conductive material into said first to third contact openings; and

connecting said first and third diffusion regions to first and third bit lines disposed on a layer overlying said semiconductor substrate, respectively, and

connecting said second diffusion region to a second bit line

disposed on said layer overlying said semiconductor substrate via a contact.

33. The method according to claim 32, further comprising the step of:

forming an impurity region at an end portion of at least one of said first diffusion region in the semiconductor substrate immediately under said first gate electrode and said third diffusion region in the semiconductor substrate immediately under said second gate electrode, said impurity region being of a same polarity as any of said diffusion regions and a low concentration than said diffusion regions.

34. The method according to claim 32, further comprising the step of:

forming an impurity region of a polarity opposite that of said diffusion regions, in said semiconductor substrate between said first and second diffusion regions immediately under said first gate electrode and /or, in said semiconductor substrate between said second and third diffusion regions immediately under said second gate electrode.

35. A method of manufacturing a semiconductor memory device comprising the steps of:

forming an insulating film on a semiconductor substrate and first and second gate electrodes on the insulating film and forming impurity regions with a relatively low concentration with said first and second gate electrodes patterned as masks, said first and second gate electrodes being adjacent to each other,

said impurity regions with said relatively low concentration being formed in at least first and third regions among said first region located on one side of said first gate electrode, a second region located

between said first gate electrode and said second gate electrode located on an opposite side to said one side of said first gate electrode, and said third region located on an opposite side to said second region for said second gate electrode;

forming a second diffusion region in said second region between said first and second gate electrodes adjacent to each other;

forming an impurity region of a polarity opposite that of said second diffusion region at an end portion of said second diffusion region in said semiconductor substrate immediately under at least one gate electrode of said first and second gate electrodes;

depositing an insulating film over said semiconductor substrate and removing the insulating film by etch-back, thereby to form spacers made of the insulating film on side walls of said first and second gates; and

forming first and third diffusion regions in said first region and said third region in said semiconductor substrate, respectively;

wherein first and third impurity regions with a relatively low concentration are provided adjacent to said first and third diffusion regions and immediately under the spacers on the side walls of said first and second gates respectively,

said method further comprising the step of:

depositing a metal film over said semiconductor substrate to form silicide layers on a surfaces of said gate electrodes and said diffusion regions;

wherein a memory cell transistor including said first and second

diffusion regions, the insulating film under said first gate electrode, and said first gate electrode constitutes a first memory cell,

a memory cell transistor including said second and third diffusion regions, the insulating film under said second gate electrode, and said second gate electrode constitutes a second memory cell, and

said first and second gate electrodes are connected in common to form a word line,

said method further comprising the steps of:

depositing an insulating film over said semiconductor substrate and opening first to third contact openings at locations associated respectively to said first to third diffusion regions;

filling a conductive material into said first to third contact openings; and

connecting said first and third diffusion regions to first and third bit lines disposed on a layer overlying said semiconductor substrate, respectively, and connecting said second diffusion region to a second bit line disposed on said layer overlying said semiconductor substrate via a contact.

36. A method of manufacturing a semiconductor memory device comprising the steps of:

forming an insulating film on a semiconductor substrate and first and second gate electrodes on said insulating film and

forming impurity regions with a relatively low concentration with said first and second gate electrodes patterned as masks, said first and second gate electrodes being adjacent to each other,

said impurity regions with said relatively low concentration being respectively formed in a first region located on one side of said first gate electrode, a second region located between said first gate electrode and said second gate electrode located on an opposite side to said one side of said first gate electrode, and a third region located on an opposite side to said second region for said second gate electrode;

forming an impurity region of a polarity opposite to those of said impurity regions at an end portion of the diffusion region immediately under at least one gate electrode of said first and second gate electrodes;

depositing an insulating film over said semiconductor substrate and removing the insulating film by etch-back, thereby to form spacers on side walls of said first and second gates; and

forming first to third diffusion regions in said first to third regions in a surface of said semiconductor substrate respectively;

first and second impurity regions of a same polarity as said diffusion regions and with said relatively low concentration being provided immediately under the spacers on the side walls of said first gate, being adjacent to said first and second diffusion regions,

third and fourth impurity regions of said same polarity as said diffusion regions and with said relatively low concentration being provided immediately under the spacers on the side walls of said second gate, being adjacent to said second and third diffusion regions,

fifth and sixth impurity regions of an opposite polarity to said second and third impurity regions being provided adjacent to said

second and third impurity regions at both ends of said second diffusion region,

said method further comprising the steps of:

depositing a metal film over said semiconductor substrate to form silicide layeres on surfaces of said gate electrodes and surfaces of said diffusion regions;

wherein a memory cell transistor including said first and second diffusion regions, the insulating film under said first gate electrode, and said first gate electrode constitutes a first memory cell,

a memory cell transistor including said second and third diffusion regions, the insulating film under said second gate electrode, and said second gate electrode constitutes a second memory cell, and

said first and second gate electrodes being connected in common to form a word line,

said method further comprising the steps of:

depositing over said semiconductor substrate an insulating film and opening first to third contact openings at locations in said first to third diffusion regions;

filling a conductive material into said first to third contact openings; and

connecting said first and third diffusion regions to first and third bit lines disposed on a layer overlying said semiconductor substrate, respectively, and connecting said second diffusion region to a second bit line disposed on said layer overlying said semiconductor substrate via a contact.

37. The method according to claim 32, further comprising the step of:

forming an impurity region at an end portion of at least one of said first diffusion region immediately under said first gate electrode and said third diffusion region immediately under said second gate electrode, said impurity region being of an opposite polarity to said diffusion regions.

38. The method according to claim 35, further comprising the step of:

forming an impurity region of an opposite polarity to said diffusion regions to be adjacent to at least one of said first impurity region provided adjacent to said first diffusion region immediately under said first gate electrode and said fourth impurity region provided adjacent to said third diffusion region immediately under said second gate electrode.